CS-00-135

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March 30, 2001

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
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Subject: Serial No. 09/759,909 01/16/01

Victor Seng Keong Lim, Feng Chen, Lap Chan, Wang Ling Goh

EXTENDED POLY BUFFER STI SCHEME

Grp. Art Unit:

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 5,506,168 to Morita et al., "Method for Manufacturing Semiconductor Device", teaches various methods of forming shallow trench isolation.

U.S. Patent 5,006,482 to Kerbaugh et al., "Forming Wide Dielectric-Filled Planarized Isolation Trenches in Semi-conductors", teaches polysilicon over oxide and etchback.

U.S. Patent 5,712,185 to Tsai et al., "Method for Forming Shallow Trench Isolation", discloses an STI process in which a polysilicon or oxide layer is used to improve the STI recessed edge.

U.S. Patent 5,229,316 to Lee et al., "Semiconductor Processing Method for Forming Substrate Isolation Trenches", teaches a STI process where a sacrificial nitride layer is formed over a polysilicon layer.

U.S. Patent 5,837,612 to Ajuria et al., "Silicon Chemical Mechanical Polish Etch (CMP) Stop for Reduced Trench Fill Erosion and Method for Formation", teaches an STI process using a polysilicon layer as a polish stop.

U.S. Patent 5,872,045 to Lou et al., "Method for Making an Improved Global Planarization Surface by Using a Gradient-Doped Polysilicon Trench-Fill in Shallow Trench Isolation", teaches filling a STI region with polysilicon.

U.S. Patent 4,307,180 to Pogge, "Process of Forming Recessed Dielectric Regions in a Monocrystalline Silicon Substrate", teaches a polysilicon layer and an etchback process to prevent dishing.

U.S. Patent 6,080,637 to Huang et al., "Shallow Trench Isolation Technology to Eliminate a Kink Effect", discloses a process for creating an insulator filled, shallow trench, in a semiconductor substrate, in which the insulator layer in the shallow trench, is not exposed to procedures used to remove defining composite insulator layers.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Sheet 1 of 1

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
CS-00-1[redacted]S	09/759-909
Applicant: Victor Seng Keong Lim et al.	
Filing Date: 01/16/01	Group Art Unit:

U. S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	5006482	4/9/91	Kerbaugh et al.	437	67	10/25/89
	6080637	6/27/00	Huang et al.	438	424	12/7/98
	4307180	12/22/81	Posse	430	314	8/22/80
	5506168	4/9/96	Morita et al.	437	67	10/11/94
	5712185	1/27/98	Tsai et al.	437	67	4/23/96
	5229316	7/20/93	Lee et al.	437	67	4/16/92
	5837612	11/17/98	Ajuria et al.	438	697	8/1/97
	5872045	2/16/99	Lou et al.	438	432	7/14/97

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

EXAMINER | DATE CONSIDERED

OIPE SC182 APR 06 2001 PATENT & TRADEMARK OFFICE